REMARKS

Applicants appreciate the examination of the present application that is evidenced by the Official Action of April 7, 2004 and the indication that Claims 28-29 and 59-62 recite allowable subject matter.

In response to the Official Action, Applicants have amended Claims 22-29 to address the section 112 rejections and have amended Claim 63 to address a claim objection. Based on these amendments, Applicants submit that the sole outstanding issues are the rejection of Claim 65 under section 112 and the rejection of Claims 22-27 and 65 under section 102(e). These rejections will now be addressed in order.

Claim 65 meets the requirements of 35 USC § 112

As described in the specification of the present application, an operation to search a CAM array block includes applying a search word (or a portion thereof) to corresponding pairs of data lines within the CAM array block. These data lines are frequently referred to as "comparand" data lines because the search word is treated mathematically as a "comparand" during a search operation. In some case, the bit lines within a CAM array block may operate as these "comparand" data lines. (See, e.g., FIG. 3A, where BIT0 and BITB0 operate as one pair of comparand data lines during search operations).

In some embodiments of the present invention, the search word may be divided into a plurality of segments (e.g., xR and xS segments, or xR, xS and xT segments, etc.) and provided to the CAM array block during consecutive cycles of an instruction pipeline. For example, FIG. 6B of the application illustrates the timing of signals when a x80 search word is divided into x20 and x60 search word segments and the search operation occurs by performing a x20 search operation on the x20 segment of the CAM array block using the x20 search word segment, and then performing a x60 search operation on the x60 segment of the CAM array block using the x60 search word segment (and the results of the corresponding x20 search operation).

Now, in Claim 65, the CAM array block is recited as being configured to

support two distinct operations that are performed concurrently. The first operation includes "writing of a xR segment **of a first write word** into a first row of the CAM array block." Thus, if R=20, then 20 bits of the first write word are written into the first row of the CAM array block. The second operation involves a search of "a xS segment of the same CAM array block with **a xS segment of a first search word**." If S=60, then 60 bits of the first search word are used as a comparand to the xS segment of the CAM array block during a search operation.

Accordingly, what is being written into the first row of the CAM array block is the "**xR segment of a first write word**." Similarly, the xS segment of the CAM array block undergoes a search operation using a "**xS segment of a first search word**." As will be understood by those skilled in the art, this "search operation" means the xS segments of the stored data entries in the rows of the CAM array block are compared with a xS segment of a first search word to determine whether any of the entry segments in the rows match the corresponding segment of the search word.

In a typical scenario, the writing operation in Claim 65 may include writing the first 20 bits of an 80-bit write word (i.e., a x20 segment of a x80 write word) into a row within the CAM array block. Thereafter, during the next cycle in the instruction pipeline, the last 60 bits of the 80-bit write word (i.e., a x60 segment of the x80 write word) are written into the same row to complete a full write operation. In contrast, the concurrent search operation might include performing a x20 search of the CAM array block by applying the first 20 bits of an 80-bit search word to the data lines associated with the x20 segment of the CAM array block (e.g., leftmost 20 columns of the CAM array block) and then evaluating the high or low states of the x20 match line segments in the x20 segment of the CAM array block. (See, e.g., ML segments ML0_a (x20) and ML1_a(x20) in FIG. 6A). Then, after these partial search results have been detected, a x60 search of the CAM array block is performed using the x60 segment of the 80-bit search word.

These operations are more fully described and illustrated at TABLE 2 of the present application. In this table, the leftmost column represents time increments and the other columns illustrate the interleaved and overlapping nature of the x20

search, write or read operations with the x60 search, write or read operations.

Based on this explanation, Applicants respectfully submit that Claim 65 clearly meets the requirements of section 112. Furthermore, Applicants request the Examiner to contact the undersigned in the event any issues remain as to whether Claim 65 or the amended Claims 22-29 meet the requirements of section 112.

Claims 22-27 and 65 are Patentable over U.S. Patent No. 6,697,276

Applicants admit some confusion with the rejection of Claims 22-27 and 65 based on U.S. Patent No. 6,697,276 to Pereira et al. This is because Pereira et al. does not disclose or suggest a segmented CAM array block that can be configured to support any concurrent write and search operations. Applicants acknowledge that FIG. 31 of Pereira et al. illustrates a "hash CAM block" **470**. But, this hash CAM block **470** does not use a segmented CAM array block as argued by the Examiner. Instead, it uses the segmented memory array **477** in FIG. 31, which represents a conventional memory array which does not utilize any CAM cells.

In order to perform a search operation in the hash CAM block **470**, the search key SKEY **210** is provided to an output logic circuit **475** along with a "read" word that has been read from the segmented memory array **477**. This "read" word is obtained by supplying a read address to the address decoder **195** and the performing a conventional read operation within the memory array **477**. The output logic circuit **475** illustrated by FIG. 32 of Pereira et al. includes compare logic $\mathbf{135_1}$ - $\mathbf{135_4}$. This compare logic compares the search key SKEY **210** with the "read" word that has been obtained from the memory array **477** and generates a search result.

Accordingly, when the hash CAM block **470** undergoes a "search" operation, the memory array **477** actually undergoes a read operation to obtain a single "read" word from an addressed row within the memory array **477**. Only after this read operation is performed, is a comparison operation performed in the compare logic $\mathbf{135_1}$ - $\mathbf{135_4}$ of FIG. 32 to complete the search operation.

Thus, it cannot reasonably be maintained that Pereira et al. discloses or

suggests any type of CAM array block that can concurrently support segmented write and search operations, or segmented read and search operations, or segmented write, search and read operations, as claimed in the present application. Instead, the memory array **477** at FIG. 31 of Pereira et al. can only support a conventional read operation or a write operation by accessing the address decoder **195**. The memory array **477** cannot support any search operation because the memory array **477** does not contain any CAM cells that would support such a search operation. Indeed, if anything, Pereira et al. actually teaches away from the present invention by arguing that CAM array blocks are less preferred because they require too much layout area. This is because each CAM cell in each row of the CAM array block requires its own internal compare circuit. (See, e.g., Pereira et al., Col. 1, lines 50-60).

Based on these arguments, Applicants respectfully request passing all pending claims to issuance. **In addition, Applicants request acknowledgment of the references cited on the attached electronic IDS, which was previously submitted to the Patent Office on March 15, 2004 and confirmed by electronic receipt.**

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 14, 2004.

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